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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,213	02/01/2002	Peter G. Hartwell	10006165-1	5663

7590 11/10/2003

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EXAMINER	
MALDONADO, JULIO J	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 11/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,213	HARTWELL ET AL.	
	Examin r	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *10-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-9 in Paper file don 09/16/2003 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Kneezel et al. (U.S. 6,436,793 B1).

In reference to claim 1, Kneezel et al. (Figs.1-10) in a related method to form a die assembly teach providing a wafer stack defining a plurality of die assemblies (32, 34), the wafer stack having a first wafer (10) and a second wafer (20), a first die assembly of the plurality of die assemblies (32, 34) being formed of at least a portion of the first wafer (10) and at least a portion of the second wafer (20); exposing a portion of the first wafer (10) by removing a portion of the second wafer (20); and dicing the exposed portion of the first wafer (10) such that the first die assembly is at least partially separated from the wafer stack (column 4, line 16 – column 9, line 8).

In reference to claim 2, Kneezel et al. teach wherein the first wafer and the second wafer are arranged in an overlying relationship with each other and bonded together to form the wafer stack (Fig.5).

In reference to claim 3, Kneezel et al. inherently teach wherein the first wafer includes a first component, the first component being arranged adjacent to the second wafer, the first component being configured to electrically communicate with a component external to the wafer stack (column 1, lines 10 – 39).

In reference to claim 4, Kneezel et al. teach wherein the wafer stack includes a third wafer, the second wafer being arranged at least partially between the first wafer and the third wafer; and wherein the step of exposing a portion of the first wafer comprises the step of exposing a portion of the first wafer by removing a portion of the third wafer and a portion of the second wafer (column 9, lines 1 – 15).

In reference to claim 5, Kneezel et al. teach wherein the step of exposing a portion of the first wafer comprises the steps of dicing the second wafer to enable detachment of a portion of the second wafer from the wafer stack; and removing the portion of the second wafer from the wafer stack (column 6, lines 7 – 63).

In reference to claim 6, Kneezel et al. teach wherein the step of dicing the exposed portion of the first wafer comprises the step of performing a through-cut of the wafer stack to at least partially detach the first die assembly from the wafer stack (column 6, lines 7 – 63).

In reference to claim 7, Kneezel et al. teach wherein the second wafer defines a recessed portion, the recessed portion being arranged in an overlying relationship with

the first component, the recessed portion being configured to enable a partial through-cut of the second wafer in a vicinity of the recessed portion such that the first component is not damaged during formation of the primal through-cut; and wherein the step of exposing a portion of the first wafer comprises the step of performing a partial through-cut of the second wafer in the vicinity of the recessed portion such that the first component is not damaged by the partial through-cut (column 6, lines 7 – 63).

In reference to claim 8, Kneezel et al. teach wherein the step of exposing a portion of the first wafer comprises the steps of exposing a portion of the second wafer by removing a portion of the third wafer; and exposing a portion of the first wafer by removing a portion of the second wafer (column 9, lines 1 – 15).

In reference to claim 9, Kneezel et al. teach wherein the step of dicing the second wafer comprises the step of performing a first partial through-cut and a second partial through-cut of the wafer stack to at least partially detach of a portion of the second wafer from the wafer stack, the portion of the second wafer to be detached being arranged between the first partial through-cut and the second partial through-cut (column 6, lines 7 – 63).

Conclusion

4. Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November

1989). The Art Unit 2823 Fax Center number is **(703) 305-3432**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at **(703) 306-0098** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via julio.maldonado@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

JMR
10/27/03

George Fourson
Primary Examiner